[moved] moves to a third predetermined level in response to the plurality of phase generators during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and [a] second gating devices, during the first and second phases, respectively.

3. (Once Amended) A charge pump, comprising:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively; and

wherein the first and second main pump capacitors [is] are prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level [moved] moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level is [moved] moves to a third predetermined level in response to the plurality of phase generators during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and [a] second gating devices, during the first and second phases, respectively.

5. (Once Amended) A charge pump, comprising:

an oscillator to generate a first and a second phase during a phase cycle;

a primary phase generator coupled to the oscillator;

a secondary phase generator coupled to the primary phase generator;

first and second preboot capacitors coupled to the primary phase generator;

first and second main pump capacitors coupled to the secondary phase generator, and the first and second preboot capacitors, respectively;

first and second gating devices coupled to the first and second main pump capacitors, respectively; and

wherein the first and second main pump capacitors [is] are prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level [moved] moves to a second predetermined level in response to the primary phase generator during the first and second phases, respectively, wherein the second predetermined level is [moved] moves to a third predetermined level in response to the secondary phase generator during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and [a] second gating devices, during the first and second phases, respectively.

19. (Once Amended) A charge pump, comprising:

an oscillator to generate a first and a second phase during a phase cycle;

a primary phase generator coupled to the oscillator;

a secondary phase generator coupled to the primary phase generator;

first and second preboot capacitors coupled to the primary phase generator;

first and second main pump capacitors coupled to the secondary phase generator, and the first and second preboot capacitors, respectively;

first and second gating devices coupled to the first and second main pump capacitors, respectively; and

wherein the first and second main pump capacitors [is] are prebooted to a first predetermined level of approximately in the range of about 1 to 5 volts by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level [moved] moves to a second predetermined level of approximately in the range of about 1 to 5 volts in response to the primary phase generator during the first and second phases, respectively, wherein the second predetermined level is [moved] moves to a third predetermined level of approximately in the range of about 1 to 1.5 volts in response to the secondary phase generator during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and [a] second gating devices, during the first and second phases, respectively.

20. (Once Amended) A charge pump, comprising:

an oscillator to generate a first and a second phase during a phase cycle;

a primary phase generator coupled to the oscillator further includes;

an inverter, coupled to the oscillator to receive an input signal from the oscillator based on the phase cycle and providing output signals which are 180 degrees out of phase; and

cross coupled gates coupled to the inverter to receive the output signals from the inverter and outputting signals that are non-overlapping and crossing around high points of their signals during the first and second phases, respectively, and further outputting signals that are non-overlapping and crossing around low points of their signals during the first and second phases, respectively;

a secondary phase generator coupled to the primary phase generator receives the signals that are non-overlapping and crossing around high points of their signals from the primary phase generator;

first and second preboot capacitors coupled to the primary phase generator receives the signals that non-overlapping and crossing around high points and low points of their signals from the primary phase generator;

first and second main pump capacitors coupled to the secondary phase generator, and the first and second preboot capacitors, respectively;

first and second gating devices coupled to the first and second main pump capacitors, respectively; and

wherein the first and second main pump capacitors [is] <u>are</u> prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level [moved] <u>moves</u> to a second predetermined level in response to the primary phase generator during the first and second phases, respectively, wherein the second predetermined level is [moved] <u>moves</u> to a third predetermined level in response to the secondary phase generator during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and [a] second gating devices, during the first and second phases, respectively.

21. (Once Amended) A charge pump, comprising:

an oscillator to generate a first and a second phase during a phase cycle;

first and second primary phase generators coupled to the oscillator;

first and second secondary phase generators coupled to the first and second primary phase generators, respectively;

first and second preboot capacitors coupled to the first and second primary phase generators, respectively;

a first main pump capacitor coupled to the first secondary phase generator, and the first preboot capacitor;

a second main pump capacitor coupled to the second secondary phase generator, and the second preboot capacitor;

a first and second p-channel gates coupled to the first and second main pump capacitors, respectively;

wherein the first main pump capacitor is prebooted to a first pre-determined level by the second preboot capacitor during the first phase, wherein the first pre-determined level [moved] moves to a second pre-determined level during the second phase in response to the first primary phase generator, wherein the second predetermined level [moved] moves to a third predetermined level in response to the first secondary phase generator, and wherein the third predetermined level dumped to a first p-channel gate during the first phase; and

wherein the second main pump capacitor is prebooted to a first pre-determined level by the first preboot capacitor during the second phase, wherein the first predetermined level [moved] moves to a second pre-determined level during the first phase in response to the second primary phase generator, wherein the second predetermined level [moved] moves to a third predetermined level in response to the second secondary phase generator, and wherein the third predetermined level dumped to a second p-channel gate during the second phase.

26. (Once Amended) A memory device, comprising:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and

the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors coupled between the first and second main pump capacitors and the first and second preboot capacitors; and

first and second gating devices coupled to the first and second main pump capacitors, respectively.

27. (Once Amended) A memory device, comprising:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second gating devices coupled to the first and second main pump capacitors, respectively; and

wherein the first and second main pump capacitors [is] are prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level [moved] moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level is [moved] moves to a third predetermined level in response to the plurality of phase generators during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and [a] second gating devices, during the first and second phases, respectively.

28. (Once Amended) A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit comprises at least one memory device, further wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors coupled between the first and second main pump capacitors and the first and second preboot capacitors; and

first and second gating devices coupled to the first and second main pump capacitors, respectively.

29. (Once Amended) A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit comprises at least one memory device, further wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors coupled between the first and second main pump capacitors and the first and second preboot capacitors; and

first and second gating devices coupled to the first and second main pump capacitors, respectively.

30. (Once Amended) A semiconductor die, comprising:

a substrate; and

an integrated circuit supported by the substrate, wherein the integrated circuit comprises at least one memory device, further wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively; and

wherein the first and second main pump capacitors [is] are prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases,

respectively, wherein the first predetermined level [moved] moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level is [moved] moves to a third predetermined level in response to the plurality of phase generators during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and [a] second gating devices, during the first and second phases, respectively.

31. (Once Amended) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors coupled between the first and second main pump capacitors and the first and second preboot capacitors; and

first and second gating devices coupled to the first and second main pump capacitors, respectively.

32. (Once Amended) A memory system, comprising:

a controller;

a command link coupled to the controller;

a data link coupled to the controller; and

a memory device coupled to the command link and the data link, wherein the memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively; and

wherein the first and second main pump capacitors [is] are prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level [moved] moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level is [moved] moves to a third predetermined level in response to the plurality of phase generators during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and [a] second gating devices, during the first and second phases, respectively.

33. (Once Amended) An electronic system, comprising:

a processor; and

at least one memory device coupled to the processor, wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively;

first and second pre-boot pre-charge capacitors coupled between the first and second main pump capacitors and the first and second preboot capacitors; and

first and second gating devices coupled to the first and second main pump capacitors, respectively.

34. (Once Amended) An electronic system, comprising:

a processor; and

at least one memory device coupled to the processor, wherein the at least one memory device comprises:

a plurality of phase generators;

first and second preboot capacitors coupled to the plurality of phase generators;

first and second main pump capacitors coupled to the plurality of phase generators, and the first and second preboot capacitors, respectively; and

first and second gating devices coupled to the first and second main pump capacitors, respectively; and

wherein the first and second main pump capacitors [is] are prebooted to a first predetermined level by the first and second preboot capacitors during the first and second phases, respectively, wherein the first predetermined level [moved] moves to a second predetermined level in response to the plurality of phase generators during the first and second phases, respectively, wherein the second predetermined level is [moved] moves to a third predetermined level in response to the plurality of phase generators during the first and second phases, respectively, and wherein the third predetermined level is dumped to the first and [a] second gating devices, during the first and second phases, respectively.

REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on June 15, 2001, and the references cited therewith.

Claims 1-3, 5, 19-21, and 26-34 are amended, as a result, claims 1- 41 are now pending in this application. The amendments to claims 2-3, 5, 19-21, 27, 30, 32, and 34 are made to correct grammatical errors and do not affect the scope of the claims. The amendments to claims 1, 26, 28, 29, 31 and 33 are fully supported by the specification as originally filed, and no new matter has been added. The amendments are made to clarify the claims and are not intended to limit the scope of equivalents to which any claim element may be entitled. Applicant respectfully requests reconsideration of the above-identified application and allowance of claims 1- 41 in view of the above amendments and remarks that follow.

Claim Objection

Claim 2 was objected to for informalities including failing to show that it has antecedent basis. Claim 2 as now amended corrects the informalities and overcomes the Examiner's